Experiment #1 - Clock and Periodic Signal Generation

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1. Clock Generation Using ICs and Analog Components
2. *Ring Oscillator*

As shown in Figure 2, propagation delay will be:

Due to the equation we have Delay = 18ns

1. *LM555 Timer*

Duty cycle and clock frequency can be calculated as below:

if :

if

if

1. Schmitt Trigger Oscillator

If R = 470then

If R = 1kthen

If R = 2.2then

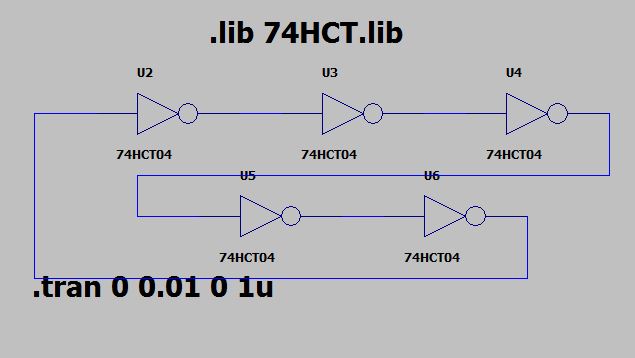
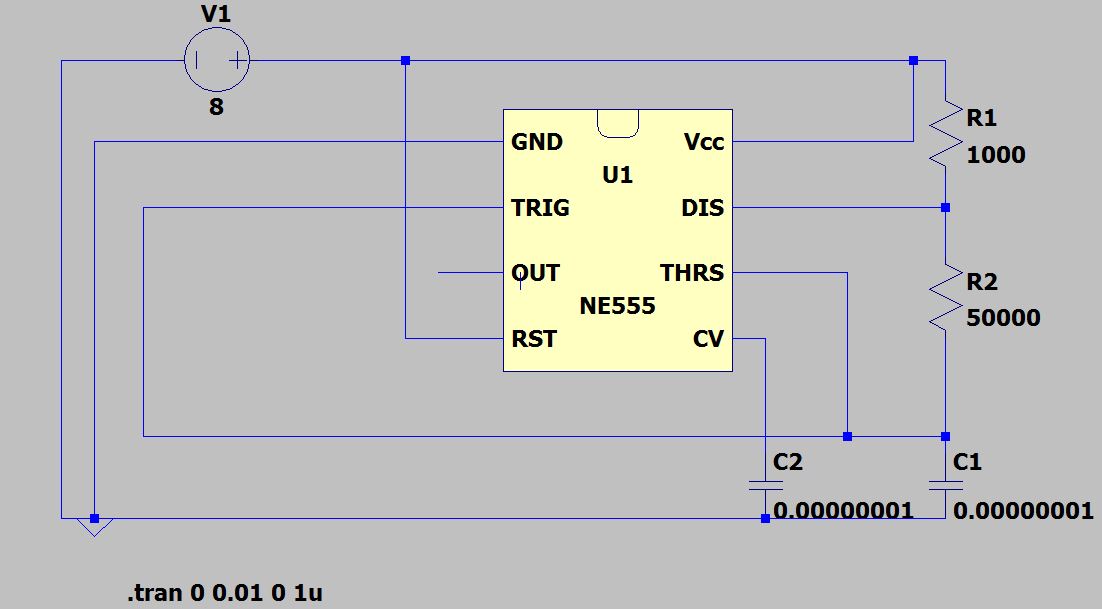
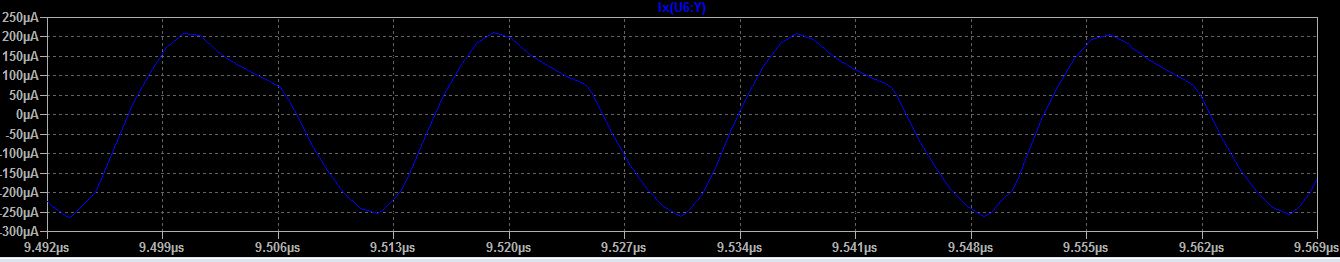
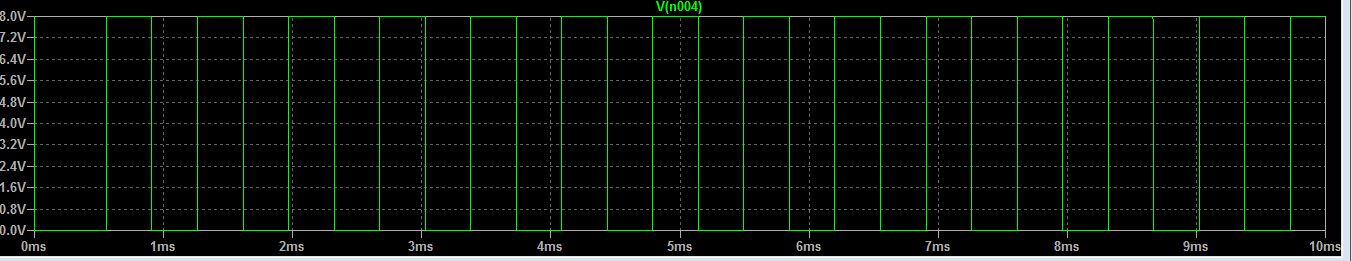


Figure 3

Figure 1

Figure 2





1. FPGA Design
2. *Ring Oscillator*

Waveform shown in Figure 4.

1. *Synchronous Counter as a Frequency Divider*

Due to Figure 5, we can see the mechanism

1. T Flip-Flop

T Flip-Flop is beside Frequency Divider in Figure 5.

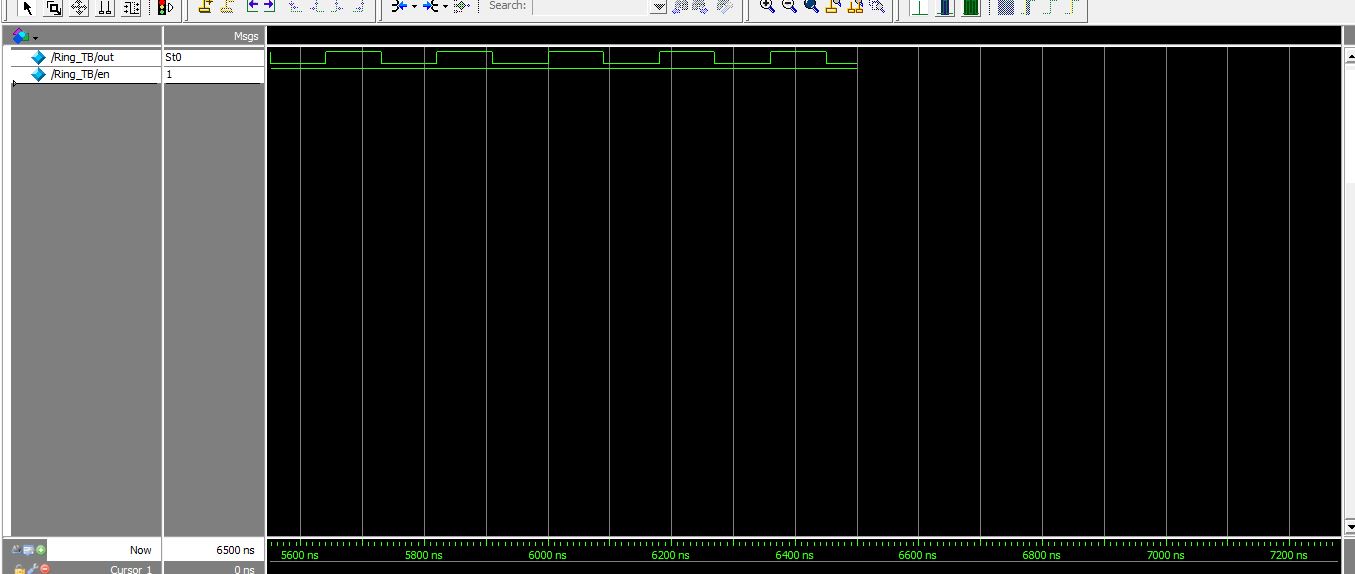


Figure 4

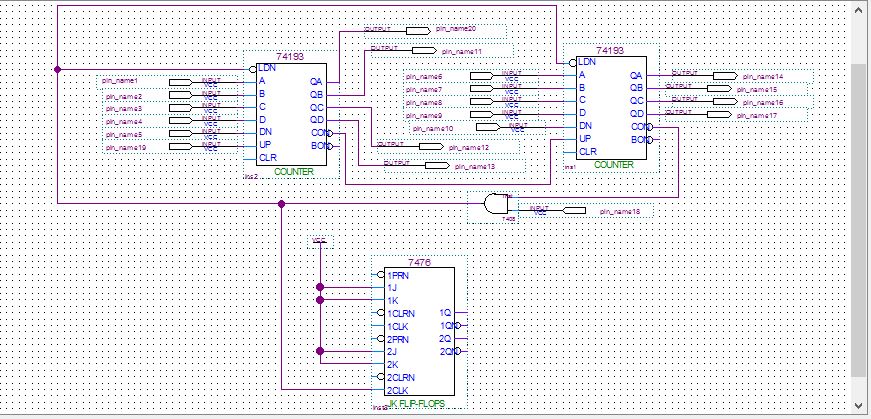


Figure 5